

Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from p-Type to n-Type Using Atomic Layer Deposition of High- κ Oxide and Its Application in CMOS Logic Circuits

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Carbon nanotubes hold great potential as channel material for thin-film transistor (TFT) applications^{1–8} due to their extraordinary electrical properties,^{9–13} such as high intrinsic carrier mobility and current-carrying capability. Compared with other popular TFT channel materials, such as polysilicon,¹⁴ amorphous silicon,¹⁵ or organic materials,^{16,17} carbon-nanotube-based TFTs have the advantages of room-temperature processing compatibility, transparency, flexibility, as well as high device performance. Nevertheless, two major challenges are still faced by carbon-nanotube-based TFTs, which are the coexistence of metallic and semiconducting nanotubes and lack of a reliable way to obtain n-type nanotube TFTs. Admixture of metallic nanotubes will lead to low on/off current ratios, and the absence of n-type TFTs will limit the applications in large-scale digital integrated circuits.

Recently, many groups including our own have demonstrated high-performance TFTs using pre-separated semiconducting nanotubes.^{18–20} However, how to obtain air-stable n-type separated nanotube TFTs (SN-TFTs) reliably still remains a big challenge. Although n-type transistors can be achieved by chemical doping^{21,22} or using metal contacts with low work functions such as Gd, Sc, or Y,^{23–25} the reliability as well as long-term air-stability of those techniques has to be further improved. Latest report shows that passivating the individual nanotube transistors using HfO₂

ABSTRACT Due to extraordinary electrical properties, pre-separated, high purity semiconducting carbon nanotubes hold great potential for thin-film transistors (TFTs) and integrated circuit applications. One of the main challenges it still faces is the fabrication of air-stable n-type nanotube TFTs with industry-compatible techniques. Here in this paper, we report a novel and highly reliable method of converting the as-made p-type TFTs using pre-separated semiconducting nanotubes into air-stable n-type transistors by adding a high- κ oxide passivation layer using atomic layer deposition (ALD). The n-type devices exhibit symmetric electrical performance compared with the p-type devices in terms of on-current, on/off ratio, and device mobility. Various factors affecting the conversion process, including ALD temperature, metal contact material, and channel length, have also been systematically studied by a series of designed experiments. A complementary metal–oxide–semiconductor (CMOS) inverter with rail-to-rail output, symmetric input/output behavior, and large noise margin has been further demonstrated. The excellent performance gives us the feasibility of cascading multiple stages of logic blocks and larger scale integration. Our approach can serve as the critical foundation for future nanotube-based thin-film macroelectronics.

KEYWORDS: carbon nanotubes · nanotube separation · thin-film transistors · atomic layer deposition · n-type transistors · CMOS integrated circuits

layer deposited by atomic layer deposition (ALD) is an effective and air-stable method to convert the devices into n-type.²⁶ Compared with other techniques, this method is relatively easy, very reliable and robust, offers long-term air-stability, and is highly compatible with the standard fabrication process adopted by semiconductor industries. However, whether this technique can be extended to nanotube TFT devices and the mechanism of such conversion still remains to be studied.

In this paper, we report our recent progress in getting n-type SN-TFTs by depositing a high- κ oxide layer onto the nanotube

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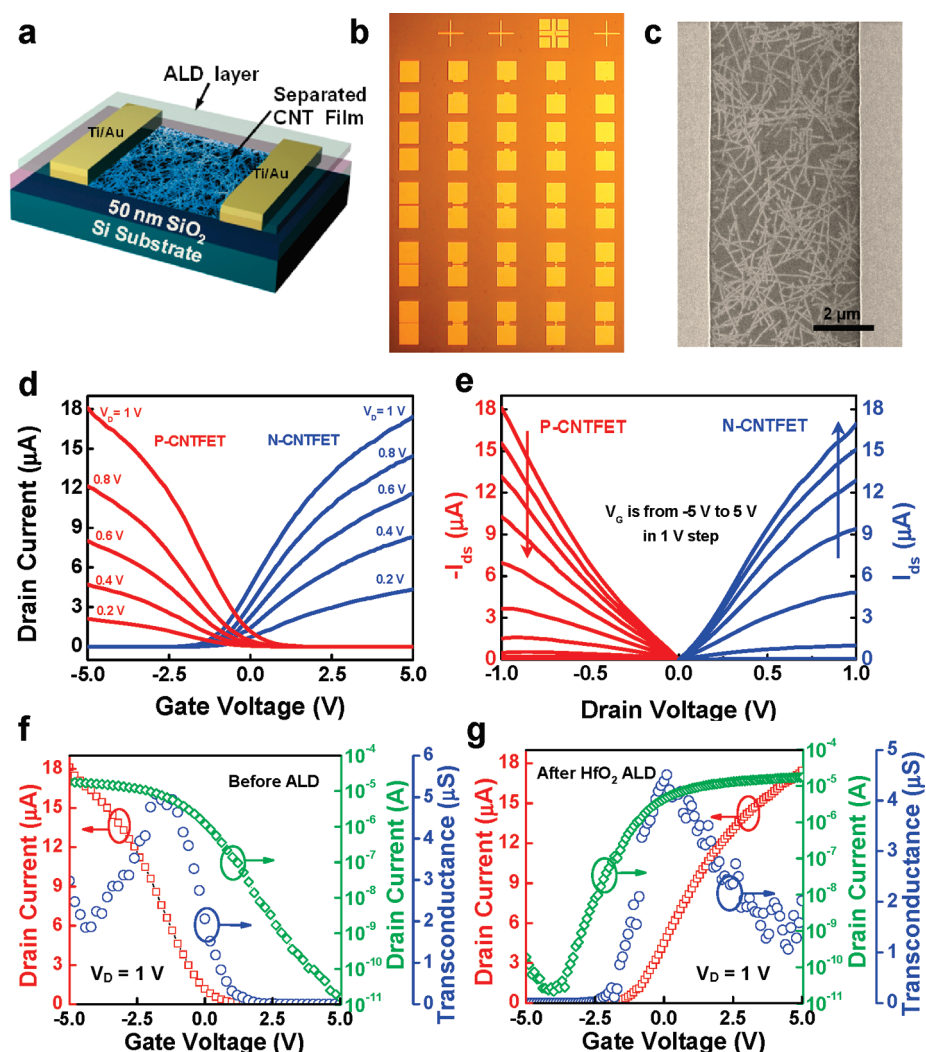


Figure 1. Symmetric p-type and n-type SN-TFTs. (a) Schematic diagram of a n-type back-gated SN-TFT with Ti/Au (5 Å/50 nm) contacts and SiO₂ (50 nm) gate dielectric. (b) Optical micrograph of the SN-TFT array with various channel lengths (5, 10, 20, 50, and 100 μm) and channel widths (10, 20, 50, 100, and 200 μm). (c) FE-SEM image of a typical SN-TFT with 5 μm channel length. (d) Transfer (I_D - V_G) and (e) output (I_D - V_D) characteristics of a typical SN-TFT ($L = 5 \mu\text{m}$, $W = 200 \mu\text{m}$) before (blue) and after (red) HfO₂ ALD. (f,g) I_D - V_G characteristics (red, linear scale; green, logarithmic scale) and g_m - V_G characteristics (blue) of the same device with $V_D = 1 \text{ V}$ before (f) and after (g) HfO₂ ALD, respectively.

surface using ALD and its applications in macroelectronic complementary metal–oxide–semiconductor (CMOS) circuits. Our work includes the following essential components. (1) Air-stable n-type SN-TFTs are obtained by passivating the back-gated transistors using a high- κ oxide layer. Such n-type devices exhibit almost perfectly symmetric electrical performance compared with the pristine p-type devices. (2) The mechanism for this carrier type conversion and the factors affecting the conversion process, including ALD temperature, metal contact material, channel length, have been systematically studied by a series of designed experiments. (3) A CMOS inverter with a maximum gain of 8.4, rail-to-rail output, symmetric input/output behavior, and large noise margin is demonstrated, which satisfies the crucial requirements for the cascading of multiple stages of logic blocks. Our CMOS SN-TFT platform shows significant

advantages over conventional platforms with respect to stability, scalability, reproducibility, and device performance and suggests a practical and realistic approach for nanotube-based CMOS integrated circuit applications.

RESULTS AND DISCUSSION

Figure 1a illustrates our n-type SN-TFT device structure. We use the solution-based aminopropyltriethoxy silane (APTES)-assisted separated nanotube deposition technique reported in our previous publication^{19,20} to deposit high density, uniform pre-separated nanotube thin film onto the Si/SiO₂ substrates. The separated nanotubes (IsoNanotubes-S) we used contain 98% semiconducting nanotubes and are obtained from NanoIntegris, Inc. The heavily doped Si substrate and 50 nm SiO₂ serve as the back-gate and gate dielectric, respectively. Au is used as the source and drain

contacts due to its favorable work function (5.1 eV), which gives similar Schottky barrier for electrons and holes, making it possible to fabricate p-type and n-type SN-TFTs with symmetric device performance. On top of the transistor, HfO_2 passivation layer is further deposited using ALD to convert the transistors into n-type. Figure 1b is a photograph showing an array of such n-type devices after fabrication. The array consists of SN-TFTs with channel widths (W) of 10, 20, 50, 100, and 200 μm and channel lengths (L) of 5, 10, 20, 50, and 100 μm . Field-emission scanning electron microscopy (FE-SEM) is used to inspect the device after the source/drain patterning, and the channel of a typical SN-TFT with 5 μm channel length is shown in Figure 1c. From the image, one can find that the channel consists of uniform and dense nanotube thin film due to the effort of our APTES-assisted deposition.

The electrical performance of the SN-TFTs is characterized. Figure 1d,e shows the family transfer (I_D-V_G) (Figure 1d) and output (I_D-V_D) (Figure 1e) characteristics of the typical SN-TFTs before (blue) and after (red) HfO_2 deposition. These curves are from the devices with the same geometry (channel length of 5 μm and channel width of 200 μm). More in-depth information of these two devices is shown in Figure 1f,g, which contain the I_D-V_G characteristics in both linear and logarithm scale and g_m-V_G characteristics measured at $V_D = 1$ V before and after HfO_2 ALD, respectively. From Figure 1d–g, one can find that the n-type SN-TFTs obtained using the ALD passivation method exhibit perfectly symmetric behavior compared with their p-type counterparts in terms of on-current (before ALD 18.1 μA , after ALD 17.4 μA), transconductance (before ALD 5.06 μS , after ALD 4.59 μS), and on/off ratio (before ALD 1.616×10^6 , after ALD 1.34×10^6). In addition, the device mobilities for these two devices are also very similar, and the typical mobilities for the devices with 5 μm channel length are about $5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ before ALD and $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ after HfO_2 ALD. Higher mobility can be obtained by increasing the device channel length as longer channel length will reduce the effect of the metal contact resistance on the device mobility. The mobility can reach 11 and $6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for p-type and n-type devices with 100 μm channel length, respectively. More information about the device mobility calculation and the n-type and p-type SN-TFT device performance metrics (I_{on}/W , on/off ratio, mobility) versus channel length can be found in the Supporting Information (Figures S1, S2).

It is worth noting that symmetric n-type and p-type transistors with good performance have also been demonstrated before by using Sc as n-type contacts and Pd as p-type contacts on an individual carbon nanotube.²⁷ Compared with the previous work, our method not only serves as an alternative approach that is compatible with the standard semiconductor fabrication process but also offers the benefit of long-

term stability in air. After being exposed in ambient conditions for 9 months, the electrical characteristics of the ALD-passivated n-type nanotube transistor remain almost unchanged, as shown in the Supporting Information (Figure S3).

To get a better understanding of such carrier type conversion, we carried out systematic experiments to study the temperature dependence of this method. HfO_2 is deposited onto the SN-TFTs using ALD at different temperatures (150 and 250 $^\circ\text{C}$). The transfer characteristics of devices with 5 μm channel length and 200 μm channel width plotted in Figure 2a clearly reveal the temperature dependence of this ALD n-type method. At low temperature (150 $^\circ\text{C}$), the device exhibits ambipolar transistor behavior, but as the temperature increases (250 $^\circ\text{C}$), the p-branch on-current decreases while the n-branch on-current increases, and the device is turned into n-type.

On the basis of the above experiments, two key factors are believed to be the reason for the conversion from pristine p-type SN-TFTs to n-type by adding ALD high- κ oxide layer: (1) the baking processing in the vacuum chamber during the ALD process, (2) the positive fixed charge in the high- κ oxide layer introduced due to the deficiency of oxygen atoms. It is known that the intrinsic carbon nanotubes have symmetric $E-k$ relationships for electrons and holes, which means that the intrinsic nanotube devices should exhibit ambipolar transistor behavior. However, the adsorption of oxygen in the ambient condition and the work function of the contact metal will affect the ultimate electrical property of the devices.^{24,28,29} For devices with Au contact, Schottky barriers are present for both the electrons and holes, but due to the adsorbed oxygen molecules, some equivalent negative charge will be stored near the source and drain contacts in the channel, which will bend the energy band upward and reduce the Schottky barrier width for holes. The bent band structures under different gate voltages are shown in Figure 2b as the dashed line. When a negative gate voltage is applied to the device, the energy band will be bent upward even further. When the Schottky barrier is thin enough, holes can tunnel through and the transistor is turned on. In contrast, when a positive voltage is applied to the gate, the energy band will be flattened, increasing the barrier for holes and putting the transistor into OFF state. Therefore, due to the presence of oxygen, the SN-TFTs with Au contact in ambient conditions typically show p-type transistor behavior.

During the ALD process, the devices are baked at 250 $^\circ\text{C}$ in an evacuated chamber with a pressure of 0.3 Torr for about 30 min. Oxygen atoms near the nanotube surface are driven away and desorbed during the ALD process. In the meantime, the high- κ oxide layer is deposited on top to passivate the device, which will prevent the oxygen from adsorbing onto the nano-

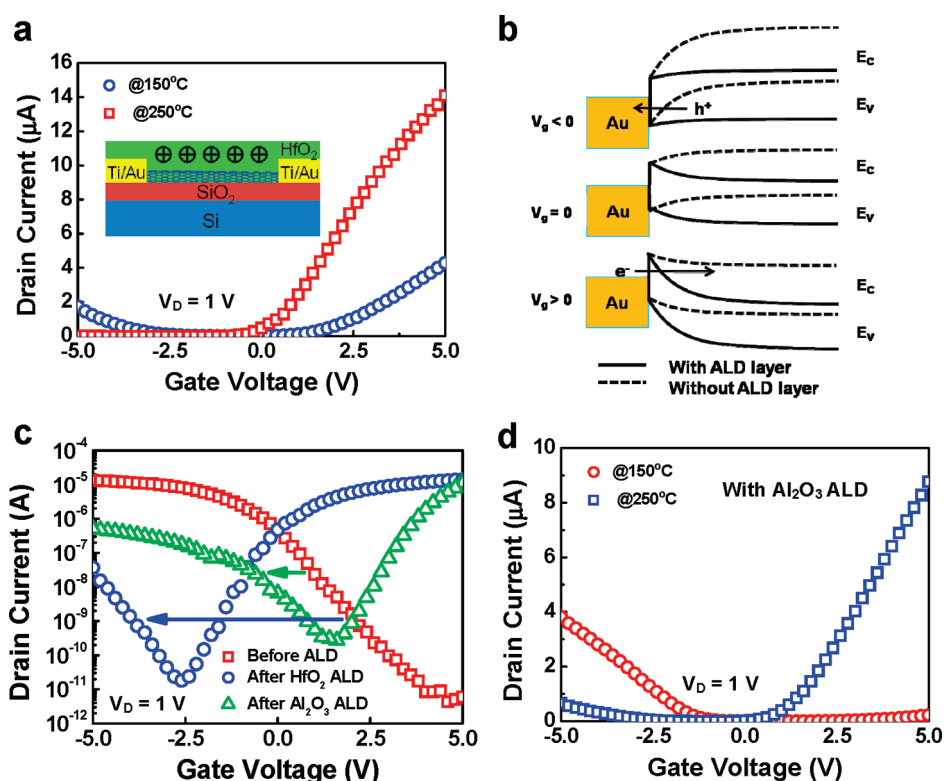


Figure 2. Mechanism of the n-type SN-TFT passivated by ALD high- κ oxide layer. (a) I_D - V_G characteristics of the SN-TFTs ($L = 5\ \mu\text{m}$, $W = 200\ \mu\text{m}$) with ALD of HfO_2 deposited at different temperatures (150 and 250°C) measured at $V_D = 1\text{ V}$. Inset: schematic diagram to explain the conversion mechanism. (b) Band structure of the nanotube-metal contact with (solid line) and without (dash line) ALD layer under different gate voltages ($V_G > 0\text{ V}$, $V_G = 0\text{ V}$, and $V_G < 0\text{ V}$). (c) I_D - V_G characteristics of a typical SN-TFT ($L = 5\ \mu\text{m}$, $W = 200\ \mu\text{m}$) in logarithm scale before (red) and after HfO_2 (blue) and Al_2O_3 (green) ALD measured at $V_D = 1\text{ V}$. (d) Temperature dependence of the I_D - V_G characteristics of the SN-TFTs ($L = 5\ \mu\text{m}$, $W = 200\ \mu\text{m}$) with ALD of Al_2O_3 measured at $V_D = 1\text{ V}$.

tube again and make the nanotube intrinsic. Moreover, positive fixed charges will also be introduced into the high- κ dielectric layer, which is supported by the capacitance-voltage (C - V) measurement by previous work,^{26,30} and the deficiency of oxygen atoms in the high- κ oxide layer is believed to be the reason for the positive charges. The generated electric field due to the accumulated positive fixed charges near the nanotube/ALD interface will bend the energy band downward and shift the transfer characteristics toward more negative gate voltages. As a result, the electron conduction is increased. Since the carrier type conversion mainly results from the charges that are close to the nanotube/ALD interface, the thickness of the ALD passivation layer should not matter that much. The corresponding energy band diagrams are shown in Figure 2b as the solid line. From the energy band, one can find that the transistor will be turned on when the gate voltage is positive and turned off when it is negative, that is, the n-type transistor behavior. When the temperature for ALD is high, the H_2O introduced during the ALD process vaporizes faster and is pumped away immediately, which means that less oxygen atoms are available during the formation of the high- κ oxide layer. As a result, due to the deficiency of the oxygen atoms in the oxide layer,

more positive charge is accumulated and the nanotube energy band will be bent down even further. This explains the temperature dependence as observed in Figure 2a.

In order to prove our hypothesis for the mechanism of the p-type to n-type conversion by the ALD high- κ oxide layer, a series of experiments are designed and carried out. We choose two p-type SN-TFTs with the same geometry and similar electrical performance and let them go through the ALD process with different high- κ materials (HfO_2 and Al_2O_3). HfO_2 ALD process is believed to introduce more positive charge than the Al_2O_3 ALD process.^{26,30} On the basis of our hypothesis, we should observe a larger shift in the transfer characteristics from the device with HfO_2 ALD than the device with Al_2O_3 ALD. The transfer characteristics of these two devices before and after ALD measured at $V_D = 1\text{ V}$ are shown in Figure 2c. The results are in accordance with the expected transistor behavior, which is good support for our hypothesis. Moreover, from the figure, one can find that the shape of the p-branch transfer characteristics of the device after ALD is very similar to the p-type transistor transfer characteristics before ALD, which is also strong evidence that the n-type transistor behavior results from the shift of

the intrinsic ambipolar behavior of SN-TFT due to the positive fixed charge.

Besides, we have also deposited Al_2O_3 onto the SN-TFTs under different ALD temperatures. Similar temperature dependence is also observed, and the transfer characteristics are exhibited in Figure 2d. The transistors covered with low-temperature ALD of Al_2O_3 still show p-type behavior, which is because the positive charge in the low-temperature Al_2O_3 layer is not sufficient to convert the device into n-type. As temperature increases, more charges are trapped in the Al_2O_3 layer, which decreases the hole conduction and increases the electron conduction. However, since Al_2O_3 provides less positive fixed charges compared with HfO_2 , the device is turned into ambipolar behavior with stronger n-branch current instead of predominant n-type. The transfer characteristics for devices with different ALD materials and various deposition temperatures are very reproducible and controllable. As a result, one can even modulate the device threshold voltage by tuning the ALD deposition condition as shown in the Supporting Information (Figure S4).

During these experiments, we have also found that channel length affects the ratio between the n-branch on-current (I_{on_N}) and p-branch on-current (I_{on_P}) of the SN-TFT after the carrier conversion. As the channel length increases, the n-branch on-current decreases more significantly than the p-branch on-current. Therefore, the $I_{\text{on}_N}/I_{\text{on}_P}$ ratio will decrease, which means that the transfer characteristics of the SN-TFTs with ALD will change from predominant n-type to almost ambipolar. This phenomenon is illustrated in Figure 3a, where devices with the same channel width ($W = 100 \mu\text{m}$) and various channel lengths ($L = 5, 10, 20, 50,$ and $100 \mu\text{m}$) are passivated with ALD of HfO_2 at 250°C . In order to get a better understanding of this channel length dependence, we measured 200 devices (100 with ALD of HfO_2 , and the other 100 with ALD of Al_2O_3), and the average ratios of $I_{\text{on}_N}/I_{\text{on}_P}$ after ALD are summarized in Figure 3b. The figure shows that both kinds of the devices have similar channel length dependence, but devices with HfO_2 passivation have much higher $I_{\text{on}_N}/I_{\text{on}_P}$ ratio than the devices with Al_2O_3 passivation.

This channel length dependence of $I_{\text{on}_N}/I_{\text{on}_P}$ is attributed to the unique feature of the nanotube network which is percolation. Unlike the aligned or individual nanotube devices,^{31,32} nanotube percolation is happening inside the channel of SN-TFTs. This gives considerable channel resistance (R_{ch}) for SN-TFTs with nanotube network as the channel material. Because $R_{\text{ch}} = R_{\square}L/W$, where R_{\square} is the sheet resistance of the separated nanotube film with a typical value of $25 \text{ k}\Omega/\square$,¹⁹ the channel resistance is directly proportional to the channel length (L). When a positive gate voltage is applied, the current is determined by the electron conductance (G_e), which equals to the inverse of the

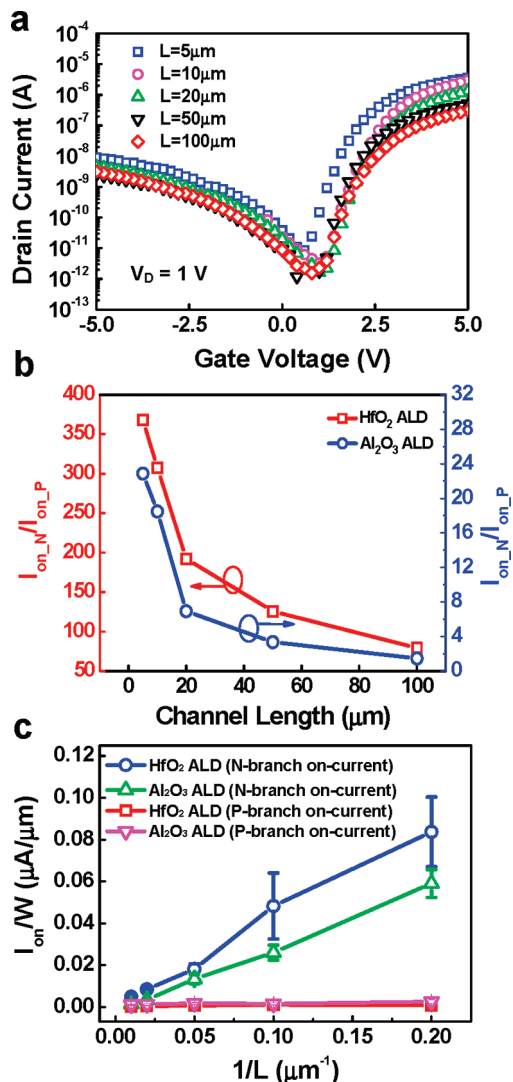


Figure 3. In-depth study of the factors affecting the n-type SN-TFT performance. (a) I_D - V_G characteristics of the SN-TFTs measured at $V_D = 1 \text{ V}$ with the same channel width ($W = 50 \mu\text{m}$) and various channel lengths ($L = 5, 10, 20, 50,$ and $100 \mu\text{m}$) plotted in logarithm scale after ALD of HfO_2 deposited at 250°C . (b) Plot of $I_{\text{on}_N}/I_{\text{on}_P}$ (the ratio between the n-branch on-current and the p-branch on-current) versus the reciprocal of channel length ($1/L$) for the n-type SN-TFTs with Al_2O_3 and HfO_2 passivation. n-Branch and p-branch on-currents are measured with $V_D = 1 \text{ V}$, $V_G = 5 \text{ V}$ or -5 V , respectively. (c) Statistical data of normalized n-branch and p-branch on-current density (I_{on}/W) versus $1/L$ for devices with HfO_2 and Al_2O_3 passivation.

sum of channel resistance and contact resistance for electrons (R_{c_e}), or we can write it as $G_e = 1/(R_{\text{ch}} + R_{c_e})$. For the n-type device, R_{c_e} is relatively small when the device is on, so when the channel length is long enough, R_{ch} will be much larger than R_{c_e} . In another word, $G_e \approx 1/R_{\text{ch}}$ and $I_{\text{on}_N} = G_e V_{\text{DS}} \approx V_{\text{DS}}/R_{\text{ch}} = V_{\text{DS}}W/R_{\square}L$, meaning that I_{on_N} is proportional to $1/L$. On the other hand, when the gate voltage is negative, the conductance for holes (G_h) can be written as $G_h = 1/(R_{\text{ch}} + R_{c_h})$, where R_{c_h} is the contact resistance for holes. For n-type devices, the contact resistance for

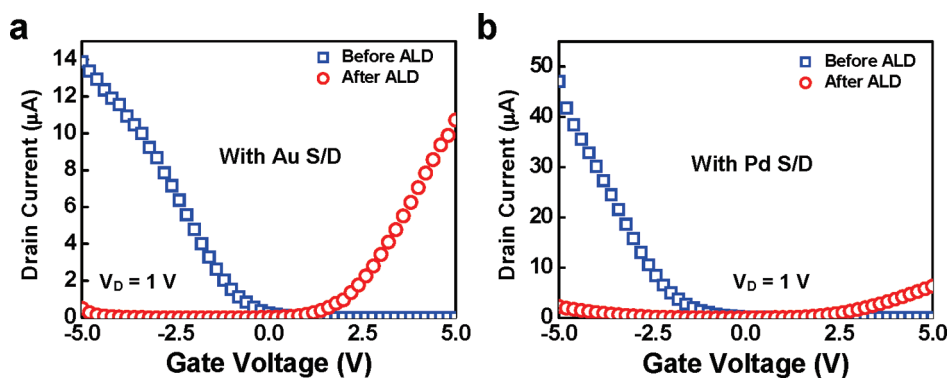


Figure 4. Effect of different source/drain metal contact materials. (a,b) I_D - V_G characteristics of typical SN-TFTs ($L = 5\ \mu\text{m}$, $W = 200\ \mu\text{m}$) with Ti/Au (a) and Ti/Pd (b) metal contacts before and after Al_2O_3 ALD measured at $V_D = 1\text{ V}$.

holes is very large even with a negative V_G because of the Schottky barrier, so $G_e \approx 1/R_{c,h}$ and $I_{on,p} = G_h V_{DS} \approx V_{DS}/R_{c,h}$. As $R_{c,h}$ comes from the Schottky barrier which is independent of L , $I_{on,p}$ will stay the same even if L varies. The statistic data in Figure 3c prove our analysis. As L increases from 5 to 100 μm , $I_{on,N}$ changes almost proportionally with $1/L$ while the variation of $I_{on,p}$ is negligible; this leads to the drop of $I_{on,N}/I_{on,p}$ ratio. Moreover, the devices covered by HfO_2 have higher $I_{on,N}/I_{on,p}$ ratio than the ones covered by Al_2O_3 because of much lower $I_{on,p}$ at the gate voltage ($V_G = -5\text{ V}$). In summary, shorter channel length and HfO_2 ALD are preferred in order to get a perfect n-type behavior transistor, which is important for integrated circuit applications as it can affect the static power consumption.

Other than the ALD temperature and channel length, the work function of the source and drain contact metal is also a crucial factor for the n-type transistor performance. For digital circuit applications, it is preferred to have symmetric p-type and n-type transistor behavior in order to simplify the circuit design and also to save the layout area. Besides, to guarantee the long-term air-stability and reliability of the n-type device performance, the source and drain metal contacts must be stable and resistant to oxidation. In this regard, some of the low work function metals such as Al and Ti *etc.* are not suitable as they will easily get oxidized under elevated temperatures during the ALD process. In comparison, Au is a good candidate as it is a stable metal and can provide similar Schottky barriers for both electrons and holes in the nanotubes, which is confirmed by the analysis using transmission line measurement (TLM) as shown in the Supporting Information (Figure S5). To verify this point, we made devices with Au and Pd as the metal contacts and converted them into n-type devices by using ALD Al_2O_3 passivation. Both kinds of devices have a channel length of 5 μm and channel width of 200 μm , and the transfer characteristics are plotted in Figure 4. The curves reveal that for the device with Pd source and drain metal contacts (Figure 4b), although the

device has a higher p-type on-current before conversion (47 μA when $V_G = -5\text{ V}$ and $V_D = 1\text{ V}$), which is what we expected as Pd forms ohmic contact for holes due to its large work function, the device after ALD has a much lower n-type on-current (6.3 μA). Moreover, after conversion, the device still has a significant amount of p-type on-current and the ratio of $I_{on,N}/I_{on,p}$ is only 2.74. In contrast, the device with Au electrodes (Figure 4a) exhibits rather symmetric device performance in terms of on-current before and after ALD (13.4 μA for the p-type device and 11.6 μA for the n-type device). Besides, after the conversion into n-type, the p-branch on-current with Au source/drain contacts is much lower compared with the device with Pd contacts and the $I_{on,N}/I_{on,p}$ ratio for this device is 43.5, 16 times larger than the Pd-contacted device. From this comparison, one can find that Au electrodes can provide symmetric p-type and n-type transistor performance and are thus better candidates than Pd for CMOS integrated circuit applications.

By utilizing the symmetric n-type and p-type SN-TFTs we have obtained, we further connect them into a CMOS inverter whose schematic is shown in Figure 5b inset. According to the discussion above, devices with 5 μm channel length, 200 μm channel width, and Au source/drain metal contacts are selected, and 15 nm ALD HfO_2 passivation deposited at 250 $^\circ\text{C}$ is used to achieve the n-type SN-TFTs. The corresponding transfer characteristics of the p-type and n-type SN-TFTs used in the inverter are shown in Figure 5a. The as-obtained CMOS inverter works with a V_{DD} of 5 V, and the corresponding inverter voltage and current transfer characteristics are plotted in Figure 5b. The inverter exhibits symmetric input/output behavior with rail-to-rail output, and the inverter threshold voltage is measured to be 2.6 V, which is very close to one-half of the supply voltage ($V_{DD}/2 = 2.5\text{ V}$). Moreover, the current is zero when the output reaches its boundary, meaning that the static power consumption is almost zero as long as the inverter stays in "0" or "1" state. In addition, by taking the derivative of the voltage transfer characteristics, one can get the information about the gain of the inverter as illustrated in Figure 5c. The highest

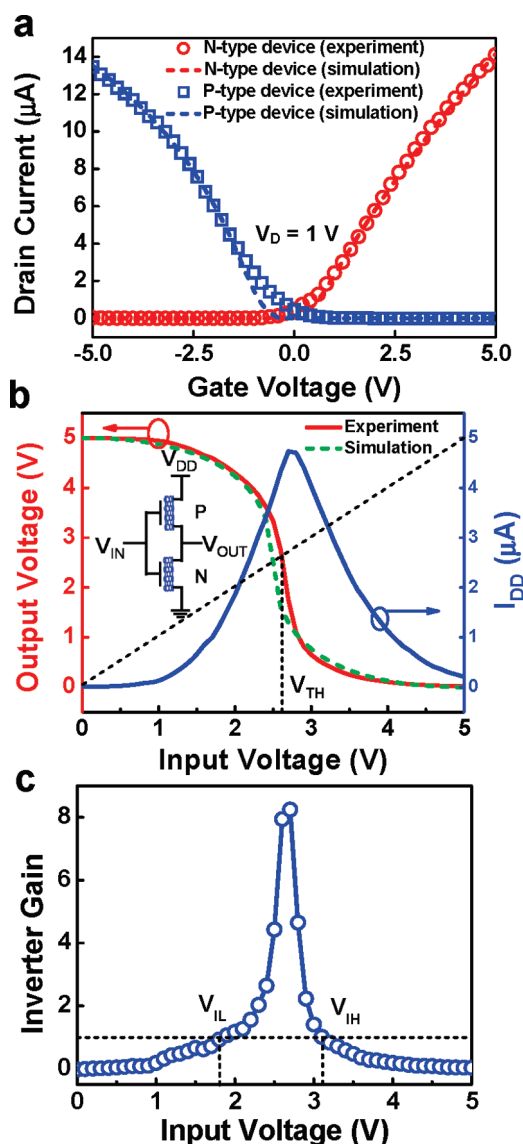


Figure 5. CMOS inverter circuit using almost symmetric p-type and n-type SN-TFTs. (a) Experiment (scatter line) and simulation (dash line) data of the I_D - V_G characteristics of typical p-type (blue) and n-type (red) SN-TFTs ($L = 5 \mu\text{m}$, $W = 200 \mu\text{m}$) used in the inverter with $V_D = 1$ V. (b) Inverter voltage (experiment, red solid trace; simulation, green dash trace) and current (blue trace) transfer characteristics. Inset: schematic diagram of the CMOS inverter. The inverter works with a V_{DD} of 5 V and exhibits symmetric input/output behavior. The inverter threshold voltage (V_{TH}) is 2.6 V. (c) Plot of inverter gain versus input voltage where the highest gain is 8.4. The input low voltage (V_{IL}) and the input high voltage (V_{IH}) are measured to be 1.8 and 3.1 V, respectively.

gain of the inverter is calculated to be 8.4 achieved at an input voltage of 2.7 V.

To make the performance of the nanotube CMOS logic circuits more predictable and practical, we utilize the compact device model based on the traditional field-effect transistor operation theory to simulate the p-type and n-type SN-TFTs as well as CMOS inverter. The model is based on the parameters such as the mobility, on/off ratio, and on-current extracted from the statistic data of 200 SN-TFTs (see Supporting Infor-

mation S1, S2), and the corresponding simulation results of the SN-TFT transfer characteristics and the CMOS inverter voltage transfer characteristics are plotted in Figure 5a,b as the dashed line, respectively. From the figure, one can find that the simulation results fit the experimental results very well, which is very important as it gives a way to simulate and predict the large-scale logic circuit performance before real circuit fabrication.

For digital circuits, other than the properties discussed above, there is one more crucial parameter affecting the circuit performance, which is the noise margin (NM).³³ It is important because it quantifies how much external signal perturbation a logic gate can withstand while operating. This tolerance ability to variations in the signal level is especially valuable for the circuit nowadays as the supply voltage is getting smaller and smaller while the parasitic effect is becoming more and more considerable. For a logic gate like an inverter, the noise margin is the minimum of two values: the noise margin for low signal levels (NM_L) and the noise margin for high signal levels (NM_H). Furthermore, NM_L is defined as the difference between maximum input voltage which can be interpreted as logic "0" (V_{IL}) and minimum output voltage when the output level is logic "0" (V_{OL}) or $NM_L = V_{IL} - V_{OL}$. Similarly, NM_H is the difference between maximum output voltage when the output level is logic "1" (V_{OH}) and minimum input voltage which can be interpreted as logic "1" (V_{IH}) or $NM_H = V_{OH} - V_{IH}$. V_{IH} and V_{IL} are usually calculated as the input voltages when the inverter gain equals to 1. Therefore, from the gain curve plotted in Figure 5c, one can find that, for our CMOS inverter, $V_{IL} = 1.8$ V and $V_{IH} = 3.1$ V. By definition, V_{OL} and V_{OH} here are 0 and 5 V, respectively, so NM_L is calculated to be 1.8 V and NM_H to be 1.9 V. Accordingly, the noise margin for the inverter is 1.8 V. As the supply voltage is 5 V and the inverter V_{TH} is 2.6 V, a noise margin of 1.8 V reveals that the circuit has very strong noise tolerance ability and is easy to cascade with other logic blocks. The reason we can get such a large noise margin is because of the contribution of both the CMOS structure and symmetric n-type and p-type transistor behavior.

In conclusion, we report a reliable method to convert the SN-TFTs into air-stable n-type transistors by passivating the devices with high- κ oxide layer deposited using ALD and its application in CMOS logic circuits. The n-type devices achieved using the proposed ALD method exhibit symmetric electrical performance as compared with the pristine p-type SN-TFTs in terms of on-current, on/off ratio, and mobility. We have further revealed that the desorption of oxygen and accumulation of positive fixed charge in the high- κ oxide layer are the reasons for the carrier type conversion, and this is verified by a series of designed experiments. Besides, we have systematically studied the factors that affect the n-type device performance including the ALD

temperature, device channel length, and the material of the source/drain metal contacts. Moreover, a CMOS inverter has been further demonstrated using p-type and n-type SN-TFTs with symmetric transistor performance. The inverter exhibits rail-to-rail output, symmetric input/output behavior, and large noise margin,

which allow the possibility of cascading multiple stages of logic gates. Our work represents a significant advance in fabricating high-performance air-stable n-type thin-film transistors using semiconducting nanotubes and can provide guidance to future research on SN-TFT-based CMOS integrated circuits.

METHODS

n-Type Separated Nanotube Thin-Film Transistor Fabrication. First, the separated nanotube thin film is deposited onto the Si/SiO₂ wafer functionalized with APTES by immersing the functionalized wafer into 0.01 mg/mL separated nanotube solution with 98% semiconducting nanotubes (NanoIntegris Inc.) for 20 min. Following the nanotube deposition is the device fabrication process. The source and drain electrodes are patterned by photolithography, and 5 Å Ti and 50 nm Au are deposited followed by the lift-off process to form the source and drain metal contacts. After source and drain patterning, because the separated nanotube thin film covers the entire wafer, in order to achieve accurate channel length and width and to remove the possible leakage between the devices, one more step of photolithography plus O₂ plasma is used to remove the unwanted nanotubes outside the device channel region. HfO₂ passivation layer is then deposited on top of the device using ALD at 250 °C. As a final step, the source and drain probing pads are opened by photolithography and wet etching.

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Supporting Information Available: Channel length dependence of n-type and p-type SN-TFT device performance metrics (S1), capacitance, mobility calculation, and channel length dependence of n-type and p-type device mobility (S2), long-term air-stability of the n-type SN-TFTs (S3), threshold voltage tuning (S4), and contact resistivity and channel sheet resistance analysis (S5). This material is available free of charge via the Internet at <http://pubs.acs.org>.

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